Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A method for timestamping events in a primary event stream, the method comprising:

receiving the primary event stream;

apportioning ~~distributing~~ events in the primary event stream among a plurality of secondary event streams; and

timestamping events in each of the plurality of secondary event streams ~~with a resolution of less than one clock cycle~~, wherein each timestamp has a first component comprising a specific clock cycle of a reference clock and a second component comprising a time at which the given event occurs within the specific clock cycle.

2. (Original) The method of Claim 1 wherein an event rate in each of the secondary event streams is lower than an event rate in the primary event stream.

3. (Original) The method of Claim 1 wherein the relative timing of the events in the primary event stream is maintained in each of the secondary event streams.

4. (Original) The method of Claim 1 wherein the primary event stream is a differential signal.

5. (Original) The method of Claim 1 wherein the secondary event streams are differential signals.

6. (Currently Amended) The method of Claim 1 wherein ~~distributing~~ apportioning events in the primary event stream comprises selectively enabling a plurality of gates such that a first event in the primary event stream passes through a first gate for generating a first one of the plurality of the secondary event streams, a second event in the primary event stream passes through a second gate for generating a second one of the plurality of the secondary event streams, and so on until an Nth event in the primary event stream passes through an Nth gate for generating an Nth one of the plurality of the secondary event streams, wherein N is a positive integer.

7. (Currently Amended) The method of Claim 1 wherein ~~distributing~~ apportioning events in the primary event stream comprises selectively enabling a plurality of gates using a counter that is clocked by the primary event stream such that a first event in the primary event stream passes through a first gate for generating a first one of the plurality of the secondary event streams, a second event in the primary even stream passes through a second gate for generating a second one of the plurality of the secondary event streams, and so on until an Nth event in the primary event stream passes through an Nth gate for generating an Nth one of the plurality of the secondary event streams, wherein N is a positive integer.

8. (Currently Amended) The method of Claim 1 wherein ~~distributing~~ apportioning events in the primary event stream comprises:

apportioning ~~distributing~~ rising edge events in the primary event stream among a first set of the plurality of secondary event streams; and

apportioning ~~distributing~~ falling edge events in the primary event stream among a second set of the plurality of secondary event streams.

9. (Original) The method of Claim 1 further comprising:

registering the events in each of the secondary event streams.

10. (Currently Amended) A timestamp system ~~circuit for timestamping events with a resolution of less than one clock cycle in a primary event stream, the circuit~~ comprising:

an event stream distributor, coupled to receive the primary event stream, for apportioning events in the primary event stream across a plurality of secondary event streams; and

a plurality of timestamp circuits, each timestamp circuit coupled to receive a respective secondary event stream from the event stream distributor, wherein each of the plurality of timestamp circuits record the times at which events occur in the respective received secondary event stream, wherein each of the recorded times have a first component comprising a specific clock cycle of a reference clock and a second component comprising a time at which the given event occurs within the specific clock cycle.

11. (Currently Amended) The timestamp system ~~circuit~~ of Claim 10 wherein an event rate in each of the secondary event streams is lower than an event rate in the primary event stream.

12. (Currently Amended) The timestamp system ~~circuit~~ of Claim 10 wherein the relative timing of the events in the primary event stream is maintained in each of the secondary event streams.

13. (Currently Amended) The timestamp system ~~circuit~~ of Claim 10 wherein the primary event stream is a differential signal.

14. (Currently Amended) The timestamp system ~~circuit~~ of Claim 10 wherein the secondary event streams are differential signals.

15. (Currently Amended) The timestamp system ~~circuit~~ of Claim 10 wherein the event stream distributor comprises:

a first counter coupled to receive the primary event stream; and

a first plurality of gates coupled to the first counter.

16. (Currently Amended) The timestamp system ~~circuit~~ of Claim 15 wherein the first counter is a Johnson counter.

17. (Currently Amended) The timestamp system ~~circuit~~ of Claim 15 wherein the first counter is an N-bit counter.

18. (Currently Amended) The timestamp system ~~circuit~~ of Claim 15 further comprising:

a second counter coupled to receive the primary event stream; and

a second plurality of gates coupled to the second counter.

19. (Currently Amended) The timestamp system ~~circuit~~ of Claim 10 further comprising:

a plurality of registers, each register operable to register events of one or more secondary event streams.

20-25. (Canceled).

26. (Currently Amended) A circuit for ~~timestamping~~ apportioning events ~~with a resolution of less than one clock cycle~~ in a signal, the circuit comprising:

a first counter coupled to receive ~~the~~ a signal having a plurality of events; and

a first plurality of gates, each gate of the first plurality of gates coupled to receive the signal ~~and each gate of the first plurality of gates coupled to receive the signal~~ and each gate of the first plurality of gates coupled to receive a respective control signal from the first counter, wherein the events of the signal are apportioned among the outputs of the first plurality of gates as a function of the respective control signal from the first counter.

27. (Original) The circuit of Claim 26 wherein the first plurality of gates are AND gates.

28. (Original) The circuit of Claim 26 wherein the signal is a differential signal.

29. (Original) The circuit of Claim 26 wherein the signal is a single-ended signal.

30. (Original) The circuit of Claim 26 wherein the first counter is a Johnson counter.

31. (Original) The circuit of Claim 26 wherein the first counter is an N-bit counter.

32. (Currently Amended) The circuit of Claim 26 further comprising:

a second counter coupled to receive the ~~primary event stream~~ signal; and

a second plurality of gates, each gate of the second plurality of gates coupled to receive the signal and each gate of the second plurality of gates coupled to receive a respective control signal from the ~~seined~~ second counter, wherein the events of the signal are apportioned among

the outputs of the second plurality of gates as a function of the respective control signal from the second counter.

33-42. (Canceled).

43. (New) The timestamp system of Claim 10, wherein the number of secondary event streams is a function of a maximum event rate in the primary event stream and a minimum period of elapse time between consecutive events for the timestamp circuit to accurately record all of the events in the primary event stream.